

MINIMUM GATE DELAY EDGE COUNTER

ABSTRACT OF THE DISCLOSURE

5 An edge counter counting both rising and falling edges
of an input signal is implemented with combinational logic,
without using flip-flops. The combinational logic is
designed using intermediate signals and state transitions
producing an output signal having a cycle corresponding to
10 a predetermined odd or even number of input signal edges,
with the logic optimized and protected against entry into
"stuck" states. A low power, low gate count edge counter
is thus implemented with an output signal duty cycle at
least as balanced as the input counter duty cycle.